IN THE CLAIMS:

Rewrite the pending claims as follows:

1. (Cancelled).

2. (Currently amended) [[The]] An output driver ~~of claim 1~~, comprising: ~~wherein said level shifter comprises:~~

an output port configured to output a data signal;

a level shifter configured to drive a current to said output port in response to an input signal;

an adjustable impedance controller configured to generate an impedance adjustment signal in accordance with topology information; and

an output impedance compensator configured to adjust the impedance of said level shifter in accordance with said impedance adjustment signal and in accordance with a reference voltage,

wherein said level shifter includes a first transistor for providing electro-static discharge protection, and wherein said first transistor has a drain terminal coupled to said output port and a gate terminal coupled to a voltage [[input]] output of [[an]] said output impedance compensator,[[;]] and a second transistor for outputting a signal with an output drive current in response to said input signal, wherein said second transistor has a drain terminal coupled to the source terminal of said first transistor, a source terminal coupled to circuit ground, and a gate terminal coupled to said input signal.

3. (Original) The output driver of claim 2, wherein the first transistor has a thicker oxide layer than the second transistor.

4. (Original) The output driver of claim 2, wherein the first transistor has a higher threshold voltage than the second transistor.

5. (Original) The output driver of claim 2, wherein said input signal comprises a plurality of pre-amplified data signals, the second transistor comprises a plurality of parallel transistors, the each having a gate connected to receive a respective one of the pre-amplified data signals.

6. (Currently amended) ~~The~~ An output driver, comprising: ~~of claim 1,~~

an output port configured to output a data signal;

a level shifter configured to drive a current to said output port in response to an input signal;

an adjustable impedance controller configured to generate an impedance adjustment signal in accordance with topology information; and

an output impedance compensator configured to adjust the impedance of said level shifter in accordance with said impedance adjustment signal and in accordance with a reference voltage;

wherein said output impedance compensator comprises:-

an operational amplifier circuit, wherein said operational amplifier circuit has a positive input terminal coupled to a reference voltage input through a first resistor, a negative input terminal coupled to circuit ground through a second resistor; and

an adjustable resistor configured to connect the output of said operational amplifier to said negative input terminal of said operational amplifier.

7. (Original) The output driver of claim 6, wherein said adjustable resistor comprises a plurality of parallel transistors configured to receive said impedance adjustment signal.

8. (Original) The output driver of claim 7, wherein the impedance adjustment signal comprises a plurality of impedance adjustment signals stored in a memory element within the adjustable impedance controller.

9. (Currently amended) The output driver circuit of claim [[1]] 2, wherein the adjustable impedance controller is configured to generate the impedance adjustment signal in response to a programmable input.

10. (Original) The output driver of claim 9, wherein the adjustable impedance controller includes a memory array and a decoder configured to access the memory array in response to the programmable input.

11. (Original) The output driver of claim 10, wherein the programmable input is based at least in part on one or more characteristics of a system in which the output driver is used.

12. (Original) The output driver of claim 9, wherein the programmable input is based at least in part on one or more characteristics of a system in which the output driver is used.

13. (Currently amended) ~~The~~ An output driver, comprising: ~~of claim 1,~~

an output port configured to output a data signal;

a level shifter configured to drive a current to said output port in response to an input signal;

an adjustable impedance controller configured to generate an impedance adjustment signal in accordance with topology information; and

an output impedance compensator configured to adjust the impedance of said level shifter in accordance with said impedance adjustment signal and in accordance with a reference voltage;

further comprising:

a tracking circuit, wherein the tracking circuit includes at least one monitor selected from the group consisting of: a process and temperature monitor, a frequency monitor, and a voltage supply monitor.

14. (Original) The output driver of claim 13, wherein

when the tracking circuit includes a process and temperature monitor, the process and temperature monitor is configured to adjust the reference voltage in response to manufacturing process and temperature variations of said output driver;

when the tracking circuit includes a frequency monitor, the frequency monitor is configured to provide a frequency component to the reference voltage in response to the frequency of the input clock signal; and

when the tracking circuit includes a voltage supply monitor, the voltage supply monitor is configured to adjust the reference voltage in accordance with an internal power supply voltage.

15. (Original) The output driver of claim 14, wherein said process and temperature monitor comprises a plurality of diodes connected in series.

16. (Original) The output driver of claim 14, wherein said frequency monitor comprises:

an input clock signal;

a current source coupled to a power supply; and

a switched capacitor circuit coupled to said current source, said switched capacitor circuit drawing an amount of current from said current source based on a predetermined frequency of said input clock signal.

17. (Original) The output driver of claim 14, wherein said voltage supply monitor comprises:

an operational amplifier having a positive terminal coupled to an internal power supply; and

a transistor having a drain terminal coupled to a current source, a gate terminal coupled to an output of said operational amplifier, a source terminal coupled to a negative terminal of the operational amplifier and to a circuit ground via a resistor.

18. (Original) An output driver comprising:

an output port;

a first transistor for configured to provide electro-static discharge protection, wherein said first transistor has a drain terminal coupled to said output port and a gate terminal coupled to an impedance compensator; and

a second transistor configured to output a signal with an output drive current in response to an input signal, wherein said second transistor has a drain terminal coupled to the source terminal of said first transistor, a source terminal coupled to circuit ground, and a gate terminal coupled to said input signal.

19. (Original) The output driver of claim 18, wherein the first transistor has a thicker oxide layer than the second transistor.

20. (Original) The output driver of claim 18, wherein the first transistor has a higher threshold voltage than the second transistor.

21. (Original) The output driver of claim 18, including a third transistor configured to provide electrical overstress protection, wherein said third transistor has a drain terminal coupled to the source terminal of said first transistor, a source terminal coupled to circuit ground, and a gate terminal coupled to an input from an electrical overstress clamp circuit.

22. (Original) The output driver of claim 18, wherein said input signal comprises a plurality of pre-amplified data signals, the second transistor comprises a plurality of parallel transistors, each having a gate connected to receive a respective one of the pre-amplified data signals.

23. (Original) The output driver of claim 18, wherein said impedance compensator comprises:

an operational amplifier circuit, wherein said operational amplifier circuit has a positive input terminal coupled to a reference voltage input through a first resistor, a negative input terminal coupled to circuit ground through a second resistor; and

an adjustable resistor configured to connect the output of said operational amplifier to said negative input terminal of said operational amplifier.

24. (Original) The output driver of claim 23, wherein said adjustable resistor comprises a plurality of parallel transistors configured to receive an impedance adjustment signal.

25. (Original) The output driver of claim 24, wherein the impedance adjustment signal comprises a plurality of impedance adjustment signals stored in a memory array.

26. (Original) The output driver of claim 18, wherein the impedance compensator comprises a circuit responsive to an impedance adjustment signal, and the output driver includes a controller configured to generate the impedance adjustment signal in response to a programmable input.

27. (Original) The output driver of claim 26, wherein the controller includes a memory array and a decoder configured to access the memory array in response to the programmable input.

28. (Original) The output driver of claim 26, wherein the programmable input is based at least in part on one or more characteristics of a system in which the output driver is used.

29. (Original) The output driver of claim 23, wherein said reference voltage is generated by a tracking circuit, the tracking circuit including at least one monitor selected from the group consisting of: a process and temperature monitor, a frequency monitor, and a voltage supply monitor.

30. (Original) The output driver of claim 29, wherein

when the tracking circuit includes a process and temperature monitor, the process and temperature monitor is configured to adjust the reference voltage in response to manufacturing process and temperature variations of said output driver;

when the tracking circuit includes a frequency monitor, the frequency monitor is configured to provide a frequency component to the reference voltage in response to the frequency of the input clock signal; and

when the tracking circuit includes a voltage supply monitor, the voltage supply monitor is configured to adjust the reference voltage in accordance with an internal power supply voltage.

31. (Original) The output driver of claim 29, wherein said process and temperature monitor comprises a plurality of diodes connected in series.

32. (Original) The output driver of claim 29, wherein said frequency monitor comprises:

an input clock signal;

a current source coupled to a power supply; and

a switched capacitor circuit coupled to said current source, said switched capacitor circuit drawing an amount of current from said current source based on a predetermined frequency of said input clock signal.

33. (Original) The output driver of claim 29, wherein said voltage supply monitor comprises:

an operational amplifier having a positive terminal coupled to said internal power supply; and

a transistor having a drain terminal coupled to a current source, a gate terminal coupled to an output and a negative input terminal of said operational amplifier, a source terminal coupled to a circuit ground via a resistor.

34. (Currently amended) An output driver comprising:

output means for outputting a data signal;

level shift means for driving a current to said output port in response to an input signal;

control means for generating an impedance adjustment signal in accordance with topology information; and

compensator means for adjusting the impedance of said level shifter in accordance with said impedance adjustment signal and in accordance with a reference voltage;

wherein said level shift means includes a first transistor means for providing electro-static discharge protection, and wherein said first transistor means is coupled to a voltage output of said compensator means, and a second transistor means for outputting a signal with an output drive current in response to said input signal.